Atlas Procurement and Test Plan

Version: 1.2

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Doric4a and VDC

Responsibility:

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Revision History:

Version 1.0	26/1/01	First version
Version 1.1	1/2/01	Minor revisions agreed with T. Weidberg
Version 1.2	5/2/01	Minor revisions agreed with T. Weidberg

1. GENERAL INTRODUCTION

1.1 Atlas SCT Links

Data transmission to and from the Atlas SCT is done in digital form with optical links. Clock and Command signals transmitted from the counting room are received in the SCT with a pin diode. The generated signal is amplified and processed within the Doric4a chip and then passed to the FE electronics in LVDS form. In the link the data is transmitted in bi-phase mark encoded signalling. The Doric4a therefore receives this protocol recovers the BCO clock and generates the Command signal in NRZ LVDS form suitable for the ABCD FE ASICs.

Output data from the SCT is also transmitted on optical fibre. Vertical-Cavity Surface-Emitting Lasers (VCSELs) power these links driven by the VDC chip. Data is received by the chip in LVDS form and the VDC conditions the signals appropriately and generates the correct drive currents for the VCSELs.

Both of these chips are required on (or close to) the FE hybrids so have been designed to be low power, low noise and optimised for the radiation environment.

1.1.1 Doric General Description

This chip has been designed for receiving and decoding biphase mark encoded optical signals. It should be connected directly to a single PIN photodiode. In this most recent version (DORIC4a) a comparator input stage with hysteresis characteristic has been included prior to the clock and data decoding circuitry. Output is in LVDS form to cause minimal feedback to the sensitive inputs and is convenient for transmission or interfacing to other logic families.

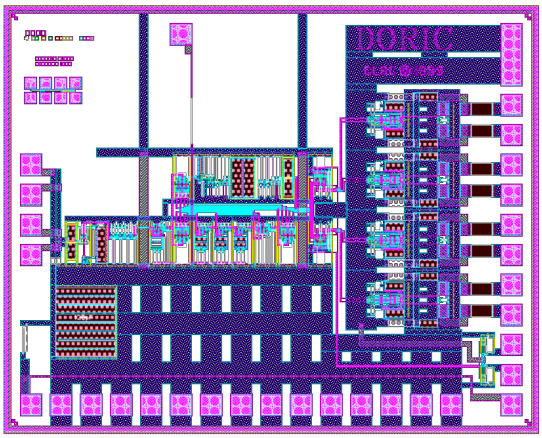

Figure 1 Doric4a Chip Layout

1.1.2 VDC General Description

This chip has been designed to drive 2 channels of vertical-cavity surface-emitting lasers. The two channels are electrically independent but share the same substrate. The circuit receives standard LVDS signalling and drives a well defined output current. The chip has been optimised for constant current draw for supply stability considerations. The chip requires a single 4V supply.

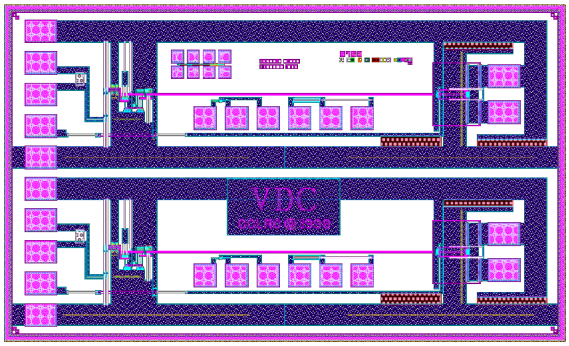

Figure 2: VDC Chip Layout

2. RADIATION QUALIFICATION

2.1 Why AMS 0.8micron BiCMOS was used

The process used to prototype the DORIC and VDC front-end opto-interface circuits for ATLAS is not qualified as a radiation hard process. An attempt was made to produce radiation tolerant devices by design i.e. by component selection, choice of operating conditions, type of circuitry used and careful layout. If this exercise failed to produce sufficiently radiation tolerant devices the prototypes would still have been useful for system tests and the design could be transferred to a qualified (expensive) process.

In this case there were several points that made radiation tolerant design of these devices easier. They were simple functions, pad-bound so plenty of area was available to use good layout practice. Both designs have output stages which dominate the device power so small amounts of extra power could be used to enhance the radiation tolerance without increasing the overall power by a significant amount.

From RAL experience and the wisdom of others in printed publications, the choice of components was limited to polysilicon resistors, npn bipolar transistors and poly1-poly2 capacitors. These were the components judged to be least affected by radiation from the selection available on the AMS 0.8um BiCMOS process used for prototyping. Resistors were conservatively designed for good current rating and matching tolerance. Resistor value change was expected to be small in comparison with manufacturing tolerance. Bipolar transistors were run at a high enough emitter current density to minimise the drop in current gain caused by radiation damage. Poly1-poly2 capacitors have rather high equivalent series resistance (ESR) but this can be overcome by layout. Capacitance value change was expected to be small in comparison with manufacturing tolerance. The effects of leakage were minimised by using low-voltage, low impedance circuitry.

The circuitry was also designed to be tolerant of large component value and transistor parameter variation. Fully differential, low signal amplitude, analogue and digital circuitry was used everywhere to minimise radiation and noise effects. Complex functions were built up from numbers of small, well-defined blocks. No radiation data was available for the process so degraded parameters were estimated from published effects on similar geometry processes. Simulations were performed to test the performance with degraded transistor parameters and component tolerances, at low and high temperatures, over the full supply voltage range. The effects of parasitic components including bond wire inductance and resistance were included in simulations.

Careful layout was used to avoid creation, or turning on, of parasitic transistors. Leakage effects between components were minimised by using extra separation. All transistors were laid out with added series resistance, internally or externally, to limit the current produced by single event effects, this will not prevent occasional soft errors but should prevent single event burnout. Simple circuitry, wide separation, low-voltage operation and the epitaxial process all help to reduce the possibility of latch-up.

Because tests with prototype chips demonstrated that they were very resistant to radiation dose the designs have not been ported to guaranteed technologies. Instead it has been agreed to qualify the production wafers with a programme of testing that meets the requirements of the Atlas guidelines for such processes. Section 3 describes the agreed radiation test program.

3. RADIATION TEST PLANS

A volume of 16 wafers has been ordered. This volume is expected to satisfy the entire needs of the Atlas semiconductor tracker. Any further orders, if required, would therefore have to be qualified again with a second similar procedure.

It has been assumed that all 16 wafers delivered will originate from the same processing batch. This will be verified by scrutinising the wafer numbering. If this is not the case then the following procedure will need to be revised.

3.1 The Sample

Out of the 16 wafers:

a) Three wafers will be randomly selected. From each of those 5 working samples of each design will be taken (one from diagonal corners and one from each centre).

b) For the remaining 13 wafers one working sample of each design will be taken from each wafer.

3.2 The Test

Each selected working die will have the following exposure performed. Samples will then be re-tested to establish if any performance changes occur.

a) Exposure to a fluence of 2 10^{14} (1MeV n_{eq}) cm^{-2} at the Ljubljana reactor.

b) Exposure to a dose of 500 KGy at the Birmingham ^{60}Co source. All the ASICs will be powered during this exposure and the currents monitored.

After both types of irradiation, the ASICs will be packaged in DIL packages and the functionality tests (see Section 5) will be repeated.

4. WAFER ORDERING AND HANDLING PROCEDURES

A total of 16 wafers containing only the Doric4a and VDC chips have been ordered from AMS. These will be delivered to RAL and stored in nitrogen cabinets in building “R25 HDL”. In accordance with standard ISO9000 procedures route cards (see Appendix) will be generated that will then track the wafers. The route cards will list all procedures operated on the wafers.

4.1 Initial inspection

On reception at RAL all wafers will be inspected and stored. All number and other issues such as scratches etc will be noted on each route card.

4.2 Wafer screening

All die will be tested. The detailed procedures are described in section 5. Initially one wafer will be screened and used for initial system build. The remaining wafers will then be held until total assembly cycles have been completed. This will allow for possible refinement of procedure.

All changes to the test procedure will require a “Quality Report” form (see Appendix) to be completed by the customer.

Once the test procedures have been approved the remaining 15 wafers will be screened and data stored.

5. TEST PROCEDURE SUMMARY

All die will be exhaustively tested at wafer level. They will then go to a subcontractor for cutting and inspection prior to delivery to the Atlas harness assembly area. Each design will have a separate test rig so each wafer will be screened twice, once for each design.

The wafer tests are intended primarily as a functionality screen. There are other system performance issues that will not be tested (e.g. VDC rise-time when connected to a VCSEL). There are obvious practical reasons for this. If during the evaluation of the production links problems occur that require screening for such a parameter a new test will have to devised to cover this. Hower issues like this are expected to be dominated by the VCSEL performance and strays associated with the Kapton hybrids.

5.1 DORIC4A

5.1.1 Test Rig

The test system is a custom system developed specifically for Doric4a. It is controlled from a PC running Labview. The device under test (DUT) is connected to an interface card that drives the chip inputs and connects a digital oscilloscope for data acquisition. The DUT is driven by a custom bi-phase mark generator card and pulse generator. The system is powered by GPIB controlled power supply.

Photographs of the various parts of the system will be taken once the final test system is in place and testing is under way.

5.1.2 Test Procedure

The following steps will be followed. A good chip must pass ALL tests. If at any stage a chip violates limits listed in section 7 (Acceptance Criterion) the die is logged as bad and failure code stored in the database. Test then starts again on the next site. The testing will be carried out using Labview, which will automatically step through the following tests.

5.1.2.1 Power check

Apply 4 volts to the chip and measure current draw. Log result and compare with limits.

5.1.2.2 LVDS level check

Disable the DUT and ensure that the LVDS output levels are within the specification laid out in section 7.

5.1.2.3 Frequency synchronisation

Apply a clock to the input of the device from the bi-phase mark generator board and check to see that the output frequency is a stable 40MHz.

5.1.2.4 Clock duty cycle test

Measure the duty cycle of the output clock and check that it is within the tolerances set out on section 7.

5.1.2.5 Data decoding test

The test board used to generate the bi-phase mark encoded signal is set-up to give a data pulse out that is 3 clock cycles long, the data is to be checked to ensure that it is 3 clock cycles long and within the tolerances specified in section 7.

5.1.2.6 Channel enable test

Test that the Gate Enable functions correctly for both channels, and at the correct voltages as specified in section 7.

5.1.2.7 Secondary input test

All tests listed above have only used one of the possible inputs, this test verifies that the second input functions correctly by verifying that the clock is output correctly. As the two inputs are combined at such an early stage within the Doric4A chip it is not necessary to test the full functionality of both channels again.

5.1.2.8 35MHz and 45MHz operation

Although the Doric4A is designed to work at 40MHz it was decided to test it's operation at 35MHZ and 45MHz. Since the test system does not easily support the testing at 45MHz the following test is to be used instead.

5.1.2.9 3.5V and 4.5V supply voltage test

To simulate the testing at different speeds we will carry out the *secondary input test* again but the supply voltage will be adjusted to 3.5V to simulate lower speed operation and 4.5V to simulate higher speed operation.

5.2 VDC

5.2.1 The test rig

The test rig will consist of the probe card for making contact onto the VDC wafer, a power supply with a GPIB meter in series to measure the DUT supply current, a GPIB controlled switch box, and an oscilloscope for connecting to the outputs of the DUT to measure the voltage levels. A PC running Labview with a GPIB controller will control the system.

5.2.2 Test Procedure

The following steps will be followed. A good chip must pass ALL tests. If at any stage a chip violates limits listed in section 7 (Acceptance Criterion) the die is logged as bad and failure code stored in the database. Test then starts again on the next site.

The testing will be carried out using Labview, which will automatically step through the following tests.

5.2.2.1 Power test

Measure the supply current of the DUT then compare this with the limits laid out in section 7.

5.2.2.2 Standby current measurement

With Iset set to 4V and driving a LVDS logic zero to the chip input measure the output voltage. This voltage will be used to check that the current across the output resistor is within the specified limits.

5.2.2.3 Output Function test

Apply a LVDS signal (10KHz square wave) into input 1 of the VDC chip and with Iset set to 4V monitor the two outputs of the VDC to make sure that the currents in the output resistor are within the specifications set out in section 7. Repeat this test for input 2 disconnecting the input from the unused channel in each case.

6. DELIVERABLES

Tested cut die will be supplied to the Atlas harness assembly area. Only good die will be supplied all other die will be kept in ID for possible auditing purposes. Die will be supplied in waffle packs labelled with a numbering system that allows tray location to be mapped back to test records for possible future fault analysis.

For practical reasons route cards will not be used at die or waffle pack level. Instead electronic records will be relied on to track test data. The test engineers will ensure all data is backed up safely to more than one media system.

7. ACCEPTANCE CRITERIA

DORIC4A

Parameter Description	Lower Limit	Expected	Upper Limit	Fail Code
Chip power current	40mA	60mA	70mA	0001
LVDS level check	1V ±100mV		1.4V ±100mV	0002
Frequency synchronisation	-5%	40MHz	+5%	0003
Clk duty cycle	45%		55%	0004
Data decoding	-5nS	3 clock cycles	+5nS	0005
Gate enables	1.2V		2.8V	0006
Secondary input	-5%	40MHz	+5%	0007

VDC

Parameter Description	Lower Limit	Expected	Upper Limit	Fail Code
Iset	3.95V	4.00V	4.05V	
Chip power current	10.5mA	12.5mA	14.5mA	1001
Standby Output current	0.5mA	1.0mA	2.0mA	1002
Output High current	11.7mA	12.2mA	12.7mA	1003
Output Low current	0.5mA	1.0mA	2.0mA	1004

APPENDIX 1: Route Card

For identifying product and recording test procedures and data the “Route Card” form must be used (see sample below).

CLRC Instrumentation Department Procedure 9010 Form RC 2.0

Route Card

project	**product**	**identification**
manufacturing process / supplier		**batch ID / date**

operation	**comments**	**initial**	**date**

APPENDIX 2: QUALITY REPORT

For reporting problems with test criterion and procedures a quality report document must be completed. These are available in word format from any RAL Instrumentation person (see sample below).

CLRC Instrumentation Department — Procedure 13010, Form 2.0

Quality Report **serial number:**

Classification:	Complaint	Request For Modification	Supplier Problem	other

details of the Quality Report

raised by Originator (sign, print, date)

accepted by Quality Representative (sign, print, date)

actions agreed by Quality Representative or Quality Committee	target date	person to undertake action	completed (initial/date)

Quality Representative/Manager agreement to actions (sign, print, date)

Originator on being informed of the proposed actions (sign, print, date)