University of Oxford
Department of Physics

Project Specification

Project Name: Biphase Mark Encoder and VCSEL Drive Control Chip

Project Code: NP-ATL-ROD-BIPHASE

Group: ATLAS

Version: 2.0

Date: November 1999

Approval:

	Name	signature	Date
Project Manager	N. N. Kundu		
Originator	A. R. Weidberg		
Financial Coordinator	A. R. Weidberg		
Safety Officer			
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1.0 Project Description

1.1 Abstract

The purpose of this project is to design, fabricate and test a chip that encodes clock, L1 & slow control into one fibre channel for the ATLAS SCT front-end electronics.

1.2 Scope

To design a further iteration of the driver for clock and control optical transmission. The control data will be encoded onto the 40 MHz clock using BiPhase Mark encoding[4]. The driver chip will be optimised for driving VCSELs as the light emitter. The device must be compatible with DORIC4 [4].

2.0 Changes from previous version

There will be12 data channels in this chip instead of four in the previous version.

A new design of bi-phase mark encoding will be used for fewer jitters in the recovered clock.

New design of Mark to Space control circuit for the output for better adjustments of M/S ratio than in the previous version.

The driver for the VCSEL needs to be changed so that common cathode VCSELs can be used.

3.0 Related projects and documents

3.1 Projects

NP-ATL-FEE-ABCRDOT	ABC readout Oxford University
NP-ATL-ROD-BIPHALD	Biphase Mark Encoder and LED Drive Control Chip Oxford University BOC. TIM.

3.2 Documents

[1] DORIC, A Front End Clock and L1 Distribution Chip, J. R. Gorbold and P. Seller.
[2] ABC (Atlas Binary Chip) Project Specification, D. Campbell, RAL.
[3] DORIC4 (Digital Opto-Receiver Integrated Circuit) Project Specification , D. J. White, RAL.
[4] VDC (LED Driver Circuit) Project Specification, D. J. White, RAL.
[5] Digital Readout Chip for Silicon Strip Detectors at SDC, K. Shankar, RAL, N. Kundu, Oxford.
[7] Biphase Mark Encoder and LED Drive Control Chip, R.L. Wastie Oxford University

4.0 Technical Aspects

4.1 Requirements

4.1.1 Input Requirements

The Biphase Mark Encoder VCSEL Drive Chip (BPM) will be a twelve channel device, it will receive and encode the Trigger Timing and Control (TTC) from the TTCrx chip (RD12) "TTCrx Reference Manual". It requires an input, 40MHz Clock (CLK40) and twelve data channels, the data is 40MHz NRZ. The input data will be clocked on the positive edge of the 40MHz clock (CLK40), Fig 1.

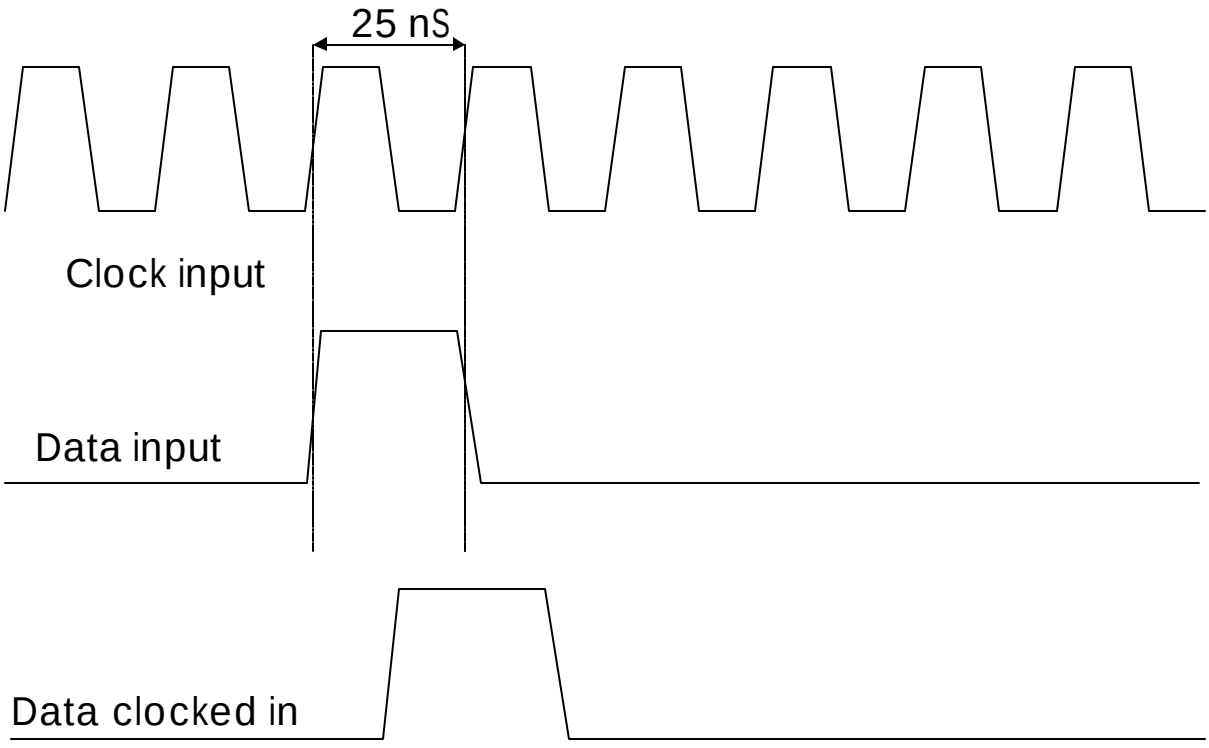

Figure 1. Input Clock and Data signals

The clock input will be PECL differential. All the other logic-input signals will be CMOS 5 volt logic (V_{IL} 0.8v MAX, V_{IH} 2v MIN) except the VCSEL driver controls which will be DC voltages in the range 0-4 volts. The BPM will be controlled by an 8-bit parallel data interface.

Table 1 Specifications for the electrical input of BPM

Rise time	<1 ns
Fall time	< 1ns
Pulse width of 20 MHz clock	12.5ns ± 250ps
Pulse width of 40 MHz clock	25ns ± 250ps
Jitter	300ps RMS
Long term drift 1 year	200ps pk-pk

BPM will have twelve VCSEL driver outputs. Each output will be capable of driving an VCSEL with its cathode connected to ground. The specifications for the electrical output of BPM are given in 2 below.

Table 2 Specifications for the electrical output of BPM

DC standing current	0.5-2.0 mA with internal resistor
Pulse current	1-16 mA set by external voltage
Rise time	<1 ns
Fall time	< 1ns
Width of 20 MHz pulse	24ns – 26ns variable
Jitter	400ps RMS
Long term drift 1 year	250ps pk-pk

The specifications for the optical output from a VCSEL (MITEL 4D469 VCSEL array) when driven by BPM are given in Table 3 below. Note that the timing specifications must be valid independently of the transition direction.

Table 3 Specifications for the optical output of a 4D469 VCSEL driven by BPM.

Rise Time	< 2 ns
Fall Time	< 3 ns
Width of 20 MHz pulse	25ns ± 500ps

Clock jitter (RMS)	< 0.5 ns
Long term drift 1 year	250ps pk-pk
Optical power coupled into 50 µm core fibre @ 16mA	> 1 mW

The BPM will encode the CLOCK and DATA for each channel and produce a Biphase Mark output, Fig 2.

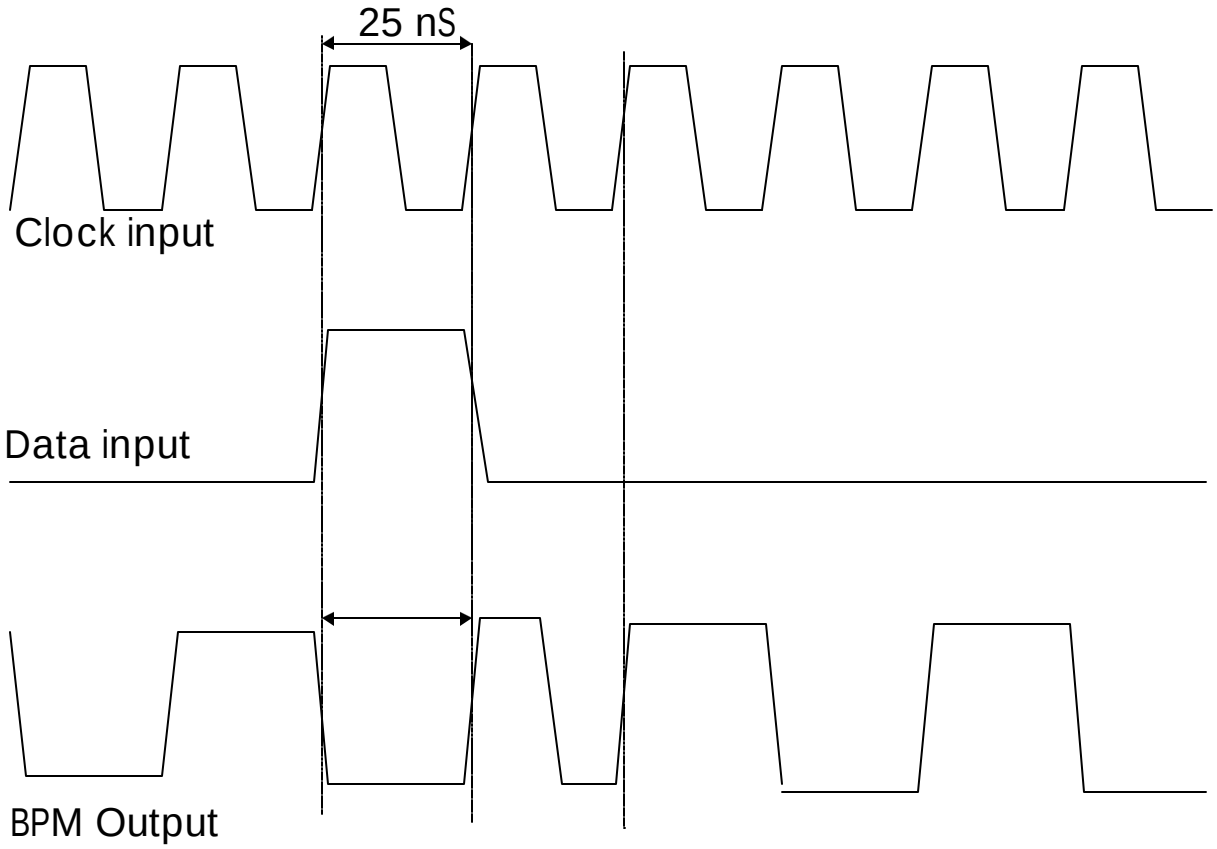

Figure 2. Biphase Mark encoded Clock & Data

4.1.3 General Requirements

1) BPM must be able to delay the input L1 trigger data by up to 32 clock cycles, and the input ATLAS timing clock in 500ps±100ps steps with a minimum range of 25ns. The delays will be programmable and setup via the parallel interface.
2) The device must have separate Digital and Analogue supplies.
3) The BPM will be required to work at ambient temperature during test and upto a

maximum of 70°C when in use on the experiment.
4) The operating temperature range will be ±5°C about nominal.
5) Supply voltages should be +5V ±0.25v for input and output stages.
6) All bond pads must have ESD protection to IEC 801-2 compliance level 2 or higher.

4.1.4 Physical Requirements

1) Bond pads or manufactured minimum size requirements should determine chip size.
2) VCSEL driver connections at one end.
3) Digital connections at the other end.
4) Package to be Quad Flat Pack.

4.2 Construction and manufacturing

The circuitry will be designed using AMS 0.8 µ BICMOS process.
Submission: December 1999

4.3 Evaluation, testing and product control

The evaluation and test will proceed in three phases
1. Electrical functionality tests and check with specification in table 2.
2. With BPM driving MITEL 4D469 VCSEL arrys the optical output will be measured with an optical probe and the signals compared to the specifications in Table 3.
3. Through the BPM chip, TTC data will be sent to DORIC4 mounted on an optoboard together with a fast epitaxial Si PIN diode. The SEQSI and LITMUS modules will be used to perform BER tests.

N.Kundu, R. Wastie, D. White, and A. Weidberg, will decide the detailed program of test at a future date.

4.4 Shipping and installation

The BPM chip will be made available to other users if needed.

4.5 Maintenance and further orders

All design information will be kept in the ATLAS archive.

5.0 Project Organisation

5.1 Personnel

Project manager:	N. N. Kundu	n.kundu1@physics.ox.ac.uk
Originator:	A. R. Weidberg	t.weidberg1@physics.ox.ac.uk
Financial Responsibility:	A. R. Weidberg	r.nickerson1@physics.ox.ac.uk

5.2 Milestones

- Final Design Review (FDR) to confirm the device as designed meet requirements of the Project Specification, including any change orders. To be arranged two weeks before submission, 3rd week of November 1999.
- BPM chip Submission 2nd December 1999.
- Concluding Review (CR) and Maintenance Review (MR) after delivery.

5.3 Deliverables

- Project documentation.
- 50 untested packaged dies

6.0 Required Resources

6.1 Manpower

6.1.1 Research Staff

N. N. Kundu Chip design 40 man/weeks

6.1.2 Nominated Technical Staff

None.

6.1.3 Design Office

None.

6.1.5 Computing

None.

6.1.6 Mechanical Workshop

None.

6.1.7 Central Electronics

None.

6.1.8 Building Services

None.

6.1.9 Physics Photographic Unit

None.

6.2 Laboratory space

One chip design seat room 468, week 22-43

6.3 Existing equipment

Chip Design Sun Workstation and software.

6.4 Cost estimate (excluding Vat)

6.4.1 Capital

None.

6.4.2 Consumables

MPW run with Europractice for prototypes for 50 packaged dies	7K
Printed circuit board and components for testing the chip.	1K
Total	8K

6.4.3 Travel

None

6.4.4 Training

None.

6.4.4 Other costs

None.

7.0 Training

None.

8.0 IPR and confidentiality

No additional IPR or confidentiality requirements beyond standard University of Oxford policy.

9.0 Safety

Low voltage, low current circuitry, no particular hazards associated with this project. Standard laser safety procedure will apply for 850nm VCSEL lasers.

10.0 Document Control

All documentation will be archived according to the ATLAS Document Management Protocol. All documents will be kept for the lifetime of the ATLAS experiment.