Project Specification

Project Name: DORIC4A

Version: 1.04

Approval:

	name	signature	date
Project Manager	**D. J. White**	**D. J. White**	**23/08/99**

Distribution for all updates:

Project Manager: D. J. White
Customer: A. R. Weidberg
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1.0 Scope

To design a further iteration of the digital optical receiver integrated circuit (DORIC4). The input stage will be modified to receive the high level, high dynamic range signal produced by a vertical-cavity surface-emitting laser (VCSEL). Comparator and decoding circuitry will be improved to assist clock and command recovery from biphase-mark encoded input signals with timing jitter and signal distortion.

2.0 Related projects and documents

ABC (Atlas Binary Chip) Project Specification, M. J. French, RAL.
Biphase Mark Encoder and LED Drive Control Chip, R. L. Wastie, Oxford Nuclear Physics.
VDC (VCSEL Driver Circuit) Project Specification, D. J. White, RAL.
Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI). Draft 1.3 IEEE P1596.3-1995.
VCSEL Tests, I. Mandic and A. Weidberg, Oxford University.

3.0 Technical Aspects

3.1 Requirements

3.1.1 General Description

DORIC4A will be a single channel device. It will receive and decode biphase-mark encoded clock and command signals. Biphase-mark encoding produces transitions corresponding to clock leading edges. Extra transitions at clock trailing edges indicate command signals. The encoding scheme is shown as figure 1.

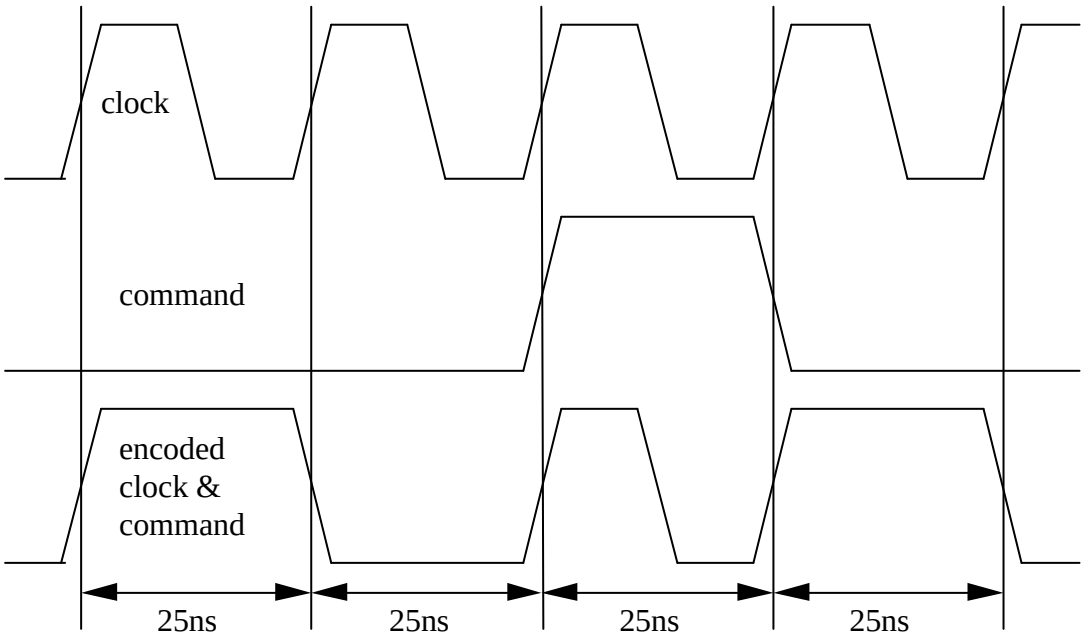

Figure 1. Biphase-mark encoded clock and command signals.

The encoded signal will drive a VCSEL to produce optical output. The high-level optical signal produced by a VCSEL will depend on its drive current, lasing threshold and efficiency. The low-level optical signal may be zero or some residual value. This optical signal is received by a PIN photodiode, which will produce an output current proportional to its optical input power. The received signal waveform and edge timing will be less perfect than the idealised version shown in figure 1. See VCSEL Tests document for more details.

3.1.2 Input Signal Level Requirements

The high-level optical signal received by the PIN photodiode should lie between 200µW and 2mW. Assuming a responsivity of 0.3A/W, the high-level signal current will lie between 60µA and 600µA. The low-level signal may be a significant percentage of the high-level signal. Assuming 33% for design purposes, the low-level signal current will lie between 0µA and 20µA for smallest signals or 0µA and 200µA for largest signals. The photodiode will also have leakage current which will increase with irradiation but this should be less than 1µA. DORIC4A must function correctly over the range of inputs shown as figure 2.

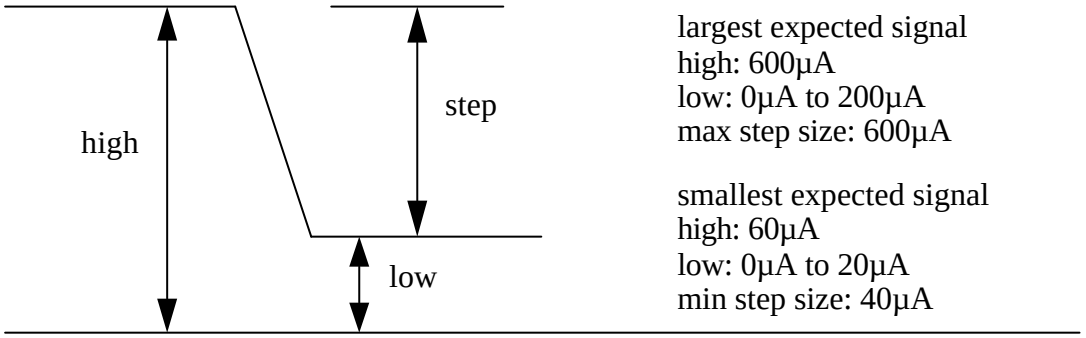

Figure 2. Input signal current amplitude range.

The smallest to largest signal operating range should be made as large as possible during circuit design. Ideally DORIC4A should work for either polarity of current to suit either polarity of PIN photodiode and/or bias voltage. The PIN photodiode and its packaging are not well characterised so DORIC4A must be designed to function correctly with a range of photodiode capacitance from 0 to 2pF and with stray capacitance of up to 4pF from each photodiode terminal to ground.

3.1.3 Noise Requirements

Total circuit noise must be low enough to guarantee a bit error rate (BER) of 10^{-11} or better, at end of life, after irradiation. This requires a signal-to-noise ratio (signal : rms noise) of 14:1 or higher (calculated from formulae by Rice, 1944 and Personick, 1973). DORIC4A must be designed to give a signal-to-noise ratio (SNR) of better than 25:1 (ratio of smallest input signal step size to internal rms noise) to allow for further degradation caused by supply noise and interference. For the large signals produced by VCSELs a high SNR is easy to achieve. Rejection of supply noise and interference will be optimised during design but there will be a practical limit to the amount of supply noise and interference which can be tolerated.
Crosstalk from data link driver outputs to DORIC4A inputs may cause large BER. The input signal amplitude may be increased to overcome this problem or data link drivers may be run at lower output current to minimise crosstalk.

3.1.4 Output Requirements

DORIC4A must decode and produce differential outputs for clock and command signals. A biphase-mark encoded input signal with jitter and/or pulse length distortion with respect to a reference clock and the decoded true clock and command outputs are shown as figure 3.

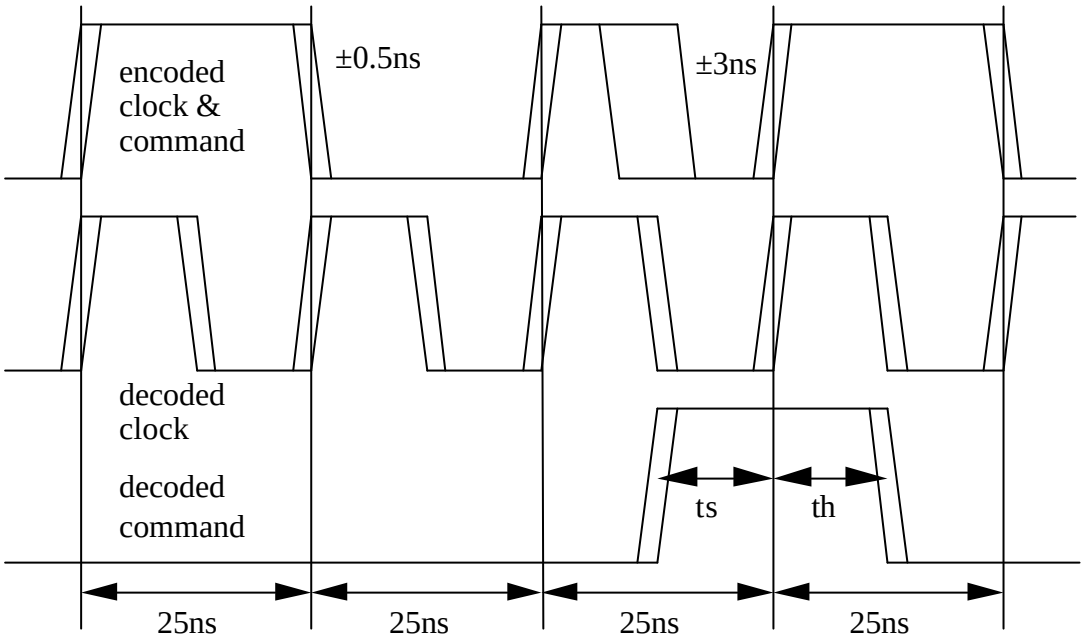

Figure 3. Worst case signal input and decoded output timing.

Clock leading edges indicated on figure 3 are produced by clock transitions of the input. Trailing edges are produced internally and are locked to leading edges. Clock output duty cycle must be close to 50%, mark and space must each be 12.5ns ± 1ns, or better. Command outputs must be one full clock cycle wide and suitably phased with respect to clock leading edges to guarantee minimum set-up and hold times (ts and th on figure 3) of 8ns for the ABC. Command outputs will be non-return-to-zero (NRZ). Input to output propagation delay of clock leading edges, nominally 8ns (not shown on figure 3 for clarity). Long term variation of propagation delay should be less than 0.5ns over lifetime.

Two sets of clock and command outputs are required, clk0 and com0, clk1 and com1. Two control inputs must be provided to enable or disable each set of outputs. Control levels for clk0 and com0 will be, low (0V ± 1V) = enable, high (+4V ± 1V) = disable. Control levels for clk1 and com1 will be, low (0V ± 1V) = disable, high (+4V ± 1V) = enable. These levels make it possible for the control signal of each module to operate the reserve/redundant output of the previous module. Control inputs will be pulled down with 20k ohm resistors so 0 outputs will be enabled and 1 outputs disabled if control signals are not connected.

Outputs will be designed to match the LVDS voltage specification. This is a balanced differential voltage output centred on 1200mV ± 75mV with a minimum signal swing of 250mV, maximum of 400mV. DORIC4A will have higher current capability than a standard LVDS output stage because the high capacitance loading of 12 ABCs plus hybrid tracking may produce very low impedance transmission lines. Rise and fall times will be made slower than a standard LVDS output stage to minimise noise injection into sensitive front end electronics. Rise and fall times, 20% to 80%, nominally 1ns.

3.1.5 General Requirements

After DORIC4A has been powered up the clock must be run for at least 10µs to allow the circuitry to settle before transmitting command signals. DORIC4A will be required to operate at an ambient temperature up to 30°C during test and down to as low as -20°C when in use on the experiment. Supply voltage +4V ± 200mV, DORIC4A must withstand an overvoltage of up to 2V without damage and function correctly, with minimal decoupling or other external components, over the specified temperature and normal supply voltage ranges. Power dissipation is dominated by the output stages. The four output drivers will use ~50mW each. The comparator and biphase mark decoding circuitry will also use ~50mW.
Any bond pads which may be attached by connectors to other modules or to long leads should aim for electrostatic discharge (ESD) protection to IEC 801-2 compliance level 2, or higher. All other bond pads to be made as well protected as possible without impairment of device performance. Careful handling will be needed to prevent damage to sensitive input pads.

3.1.6 Physical Requirements

Floor plan, figure 4.

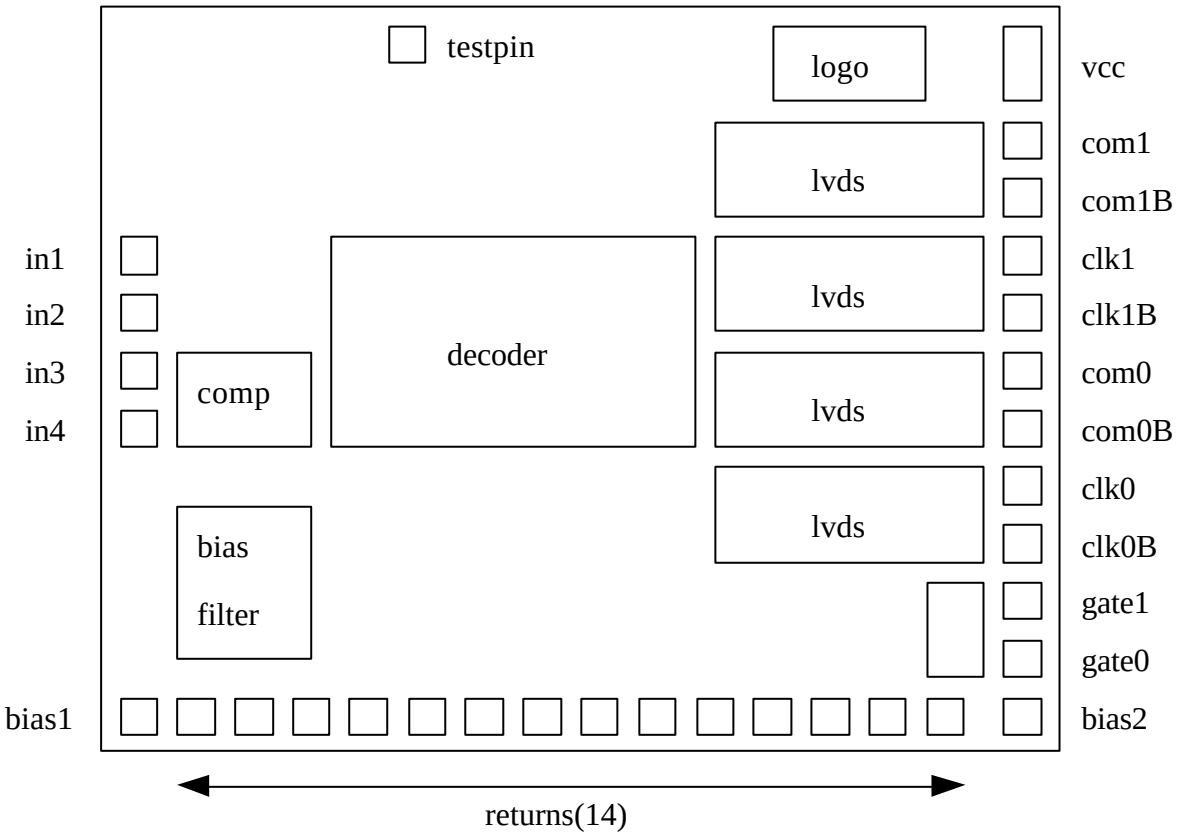

Figure 4. DORIC4A pad layout and naming.

Chip width 2.0mm, chip length 2.5mm, to fit into available space. Four input pads give balanced stray capacitance and allow reversal of the detector polarity without lead crossover.

3.1.7 Pad numbering and names

Pads are numbered in an anticlockwise direction starting at in1 for convenience.

Pad #	Name	Function
1	in1	PIN photodiode signal input, common with 4
2	in2	PIN photodiode signal input, common with 3
3	in3	PIN photodiode signal input, normal PIN diode anode
4	in4	PIN photodiode signal input, normal PIN diode cathode
5	bias1	PIN photodiode bias supply, common with 20
6-19	ret	supply return pads
20	bias2	PIN photodiode bias supply, common with 5
21	gate0	output0's enable, active low, 10k pulldown
22	gate1	output1's enable, active high, 10k pulldown
23	clk0B	LVDS clock0 output complement
24	clk0	LVDS clock0 output true
25	com0B	LVDS command0 output complement
26	com0	LVDS command0 output true
27	clk1B	LVDS clock1 output complement
28	clk1	LVDS clock1 output true
29	com1B	LVDS command1 output complement
30	com1	LVDS command1 output true
31	vcc	supply pad, large enough for several bond wires
32	testpin	dc level output of delay locked loop

Four cross-connected input pads have been supplied to avoid crossing of input bond wires if PIN connections or PIN bias require reversing.
The single vcc supply pad is large enough to take several bond wires. A minimum of two are needed to handle the supply current, more may be used to minimise inductance. A row of supply return pads has been provided. As many return pads may be bonded as are needed for good operation, six is suggested. The input signal is differential and large amplitude so there is no need for a separate analogue return.

3.2 Specification of deliverables

See Requirements.

3.3 Manufacturing

DORIC4A will be designed using AMS 0.8µm BICMOS models and design rules for fabrication on an AMS MPW run. This process is not qualified as radiation hard but, if transistors are limited to npn bipolar and if the circuitry is designed to minimise and to allow for degradation, it produces sufficiently radiation tolerant devices.

3.4 Testing and product control

A test plan has been written. These devices will be produced on a multi-project wafer so they will be delivered as small numbers of individual die. Probe testing is difficult but not impossible and is preferable to the alternatives (bonding, testing, removing and then re-bonding, or not testing at all). A conventional probe card and custom test driver will be designed and made. Some software may need to be developed.

3.5 Shipping and Installation

The customer will personally collect all of the deliverables.

3.6 Maintenance and further orders

All documentation will be kept for a period to be determined at Maintenance Review to facilitate maintenance and further orders.

4.0 Project Management

4.1 Personnel

Project manager/engineer:	D. J. White	djw@te.rl.ac.uk
Customer:	A. R. Weidberg	t.weidberg1@ph.ox.ac.uk

4.2 Deliverables

Project documentation. Test results. Application notes. Tested and untested die.

4.3 Project plan

Milestones, schedule, see also 4.4.
DORIC4 design and layout start after project specification agreed at PDR, late January 1998.
Review progress and discuss test requirements at IDR, April 1998.
Complete test plan, April 1998.
AMS 0.8µm BICMOS MPW submission after FDR, July 1998.
Produce test fixtures, equipment and software, August 1998.
Commence testing, October 1998.
Tested die required for use by November 1998.
DORIC4A design and submission following project change order and FDR, April 1999.

4.4 Design Reviews

Preliminary Design Review (PDR) to confirm the Project Specification.
Interim Design Review (IDR) to review project progress and test requirements.
Final Design Review (FDR) to confirm the devices as designed meet requirements of Project Specification, including any change orders, before submission.
Concluding Review (CR) and Maintenance Review (MR) after delivery.

4.5 Training

Minimal training requirements, short familiarisation time for latest software issue

4.6 CAE and test equipment

Workstation, software and support, to suit selected process.
Test equipment as defined in test plan.

4.7 Costs and finance

Cost of 100 prototype chips is approximately 3k pounds.
Test fixtures and components are unlikely to cost more than 1k pounds.
Finance to be arranged.

4.8 IPR and confidentiality

Instrumentation Department owns the layout and schematic databases. Any masks or phototools will be procured by the Department. None of these items will be released unless the appropriate protective agreements are in place.

4.9 Safety

Low voltage, low power circuitry, no particular hazards associated with this project.

4.10 Environmental impact

Small amounts of inert material which may be safely disposed of as landfill.