

Project Specification

Project Name: RAL232 / DRX-12

Version: 1.03

Approval:

	name	signature	date
Project Manager	D. J. White	D. J. White	09/09/99

Distribution for all updates:

Project Manager: D. J. White.

Customer: A. R. Weidberg.

Group Leader responsible for the project: M. J. French.

Project Managers of related projects: M. Goodrick.

Account Manager: W. J. Haynes.

1.0 Scope

To design a 12-channel data receiver integrated circuit (DRX) which will detect the output of an array of PIN photodiodes receiving signals from a multiple optical fibre link. Signals on the optical fibres will be produced by vertical cavity surface emitting lasers (VCSELs) driven by VCSEL driver chips (VDCs).

2.0 Related projects and documents

ABC (Atlas Binary Chip) Project Specification, M. J. French, RAL.

VDC Project Specification, D. J. White, RAL.

MITEL PIN diode package, description and specifications.

A prototype LED/PIN diode optical data link for the ATLAS semiconductor tracker,

A. Rudge et al, NIM, A 399 (1997) 119-128.

Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI).

Draft 1.3 IEEE P1596.3-1995.

3.0 Technical Aspects

3.1 Requirements

3.1.1 General Description

DRX will have 12 channels on each chip with good electrical isolation between channels to minimise crosstalk. Each channel will have an input comparator with individual threshold control and an LVDS output driver.

3.1.2 Input Requirements

Inputs will be current signals from the anodes of a common-cathode PIN photodiode array. The data format from ABC or ABCD front-end chips will be non-return-to-zero (NRZ) at 40Mbit/s. Detectors must be dc coupled to input comparators to handle the NRZ data format. DRX must have adequate bandwidth to handle data at 80Mbits/s for extra safety margin and possible alternative use. Signal currents will range from approximately 500 μ A maximum with high output VCSELs, good coupling, and no irradiation losses in fibre, to 57 μ A minimum at end of life with low output VCSELs, poor coupling and irradiation losses in fibre. See the power budget calculations produced by A. R. Weidberg, Appendix 1.

DRX must function with an input signal of 20 μ A for extra safety margin. Maximum difference in input levels between channels on a chip 3:1, not the full signal dynamic range. Crosstalk between channels must be very small to keep the bit-error-rate (BER) low. Best efforts, aiming for less than 2% channel-to-channel crosstalk.

Each channel will have an individual threshold control voltage input, nominally 0V to +2.5V giving an input signal threshold control range from 0 to 255 μ A, (1 μ A per LSB if driven by an external 8-bit DAC).

3.1.3 Output Requirements

Output signals to be LVDS compatible. Output jitter must be designed to be less than 250ps rms at 20 μ A input, less than 100ps rms for 57 μ A or larger input (assuming the input signals are stable in amplitude with variation of duty cycle). Variation of propagation delay to be minimised over signal, temperature and supply voltage ranges.

3.1.4 General Requirements

DRX will be required to operate at ambient temperatures from 0°C to 70°C. Supply voltage nominally 3.3V \pm 0.3V. DRX must function correctly over the specified temperature and supply voltage ranges and must withstand an overvoltage of at least 1V without damage.

All bond pads to be made as well protected against electrostatic discharge (ESD) as possible. It may not be possible to achieve a high degree of protection on all bond pads for reasons of noise or capacitance loading. Careful handling will be needed to prevent damage to sensitive input pads during assembly.

3.1.5 Physical Requirements

Signal input pads must be placed suitably for connection to the PIN photodiode array, with total lead length as short as possible. Signal inputs on one side of the chip, signal outputs opposite. Power, bias and threshold control signals along the remaining two sides.

3.2 Specification of deliverables

3.2.1 Functional description and application advice

The PIN photodiode array has common cathodes so the anode signals will go to single ended inputs on DRX. These inputs will be sensitive to interference noise and stray capacitance so very short, low capacitance input connections must be used.

The PIN photodiode common cathodes must be decoupled to ground close to DRX to make a good signal return path. Photodiode bias should be taken through a resistor to the cathode decoupling capacitor to filter noise from the bias supply.

Threshold inputs are 9.8k ohm to +2.5V, so the threshold driver needs to have an output stage capable of sinking 255 μ A at close to 0V.

Supply current approximately 10mA per channel at nominal supply voltage. Supply current will vary with supply voltage (+/- 10%) and the manufactured resistor tolerance (+/-15%).

Outputs are low voltage and differential but much larger than inputs so they must be routed well away from inputs. No other logic level signals may be routed near to the inputs. Noise calculations for the input stage suggest that BER and jitter will be well within specification but any interference noise reaching the sensitive inputs will degrade performance.

Treat the devices as ESD sensitive and use appropriate handling procedures until they have been assembled on to the final circuit boards.

3.2.2 Floor plan

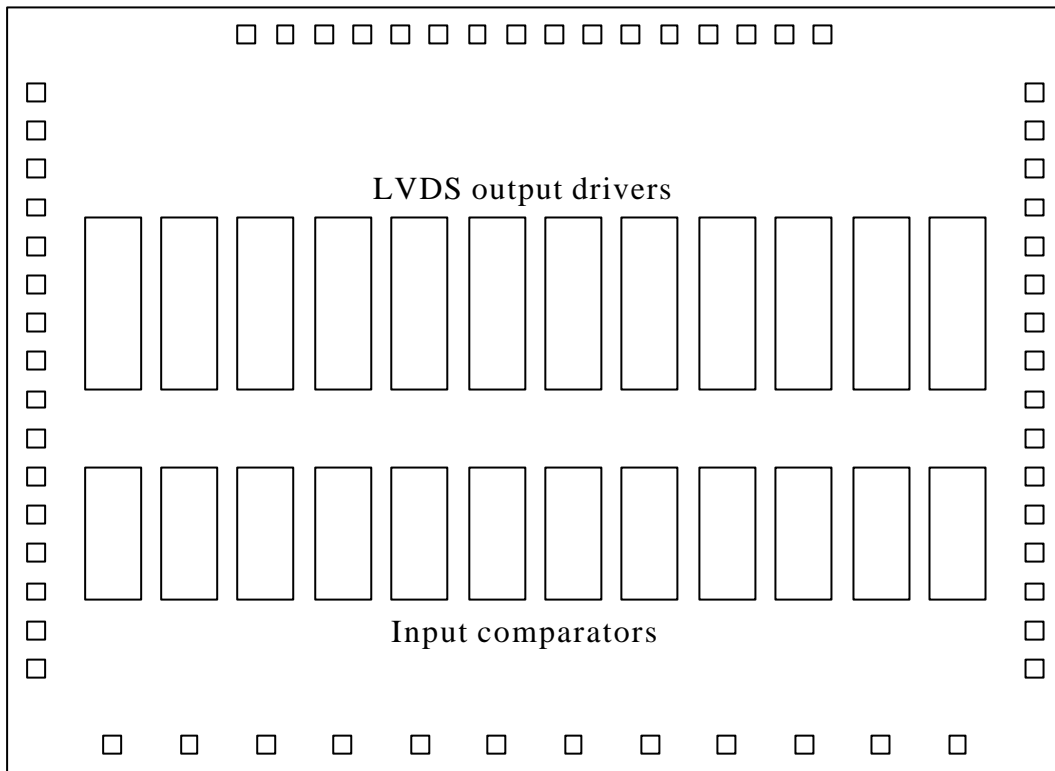


Figure 1. Floor plan of 12-channel version showing pad layout.

This 12-channel version is a simple expansion of the 4-channel prototype. It has extra supply and return pads and wider supply tracking to handle the higher total supply current.

3.2.3 Package Numbering and Names

Package pins are numbered in an anticlockwise direction starting from pin1, top, left of centre, to pin64, top, right of centre.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	O/p5b	17	VCC	33	In6	49	Return
2	O/p5	18	VCC	34	In7	50	Return
3	O/p4b	19	Thr0	35	In8	51	Return
4	O/p4	20	Thr2	36	In9	52	Return
5	O/p3b	21	Thr4	37	In10	53	O/p11b
6	O/p3	22	Thr6	38	In11	54	O/p11
7	O/p2b	23	Thr8	39	Well	55	O/p10b
8	O/p2	24	Thr10	40	N/C	56	O/p10
9	O/p1b	25	N/C	41	Thr11	57	O/p9b
10	O/p1	26	Well	42	Thr9	58	O/p9
11	O/p0b	27	In0	43	Thr7	59	O/p8b
12	O/p0	28	In1	44	Thr5	60	O/p8
13	Return	29	In2	45	Thr3	61	O/p7b
14	Return	30	In3	46	Thr1	62	O/p7
15	Return	31	In4	47	VCC	63	O/p6b
16	Return	32	In5	48	VCC	64	O/p6

All pins labelled 'Return' are taken to ground. 'Return' is used in preference to 'ground' to give more flexibility in simulation.

3.3 Manufacturing

The circuitry will be designed using AMS 0.8 μ m BICMOS models and design rules for fabrication on an AMS MPW run. Submission date 24th September 1999.

3.4 Testing and product control

Test requirements will be discussed at FDR. A test plan will be written.

Route Cards will be used to record operations such as probe test, packaging, irradiation etc. and to account for the number of chips used, lost, damaged or shipped at each operation.

3.5 Shipping and installation

The customer will personally collect all of the deliverables.

3.6 Maintenance and further orders

All documentation and test equipment will be kept for a period to be determined at Maintenance Review to facilitate maintenance and further orders.

4.0 Project Management

4.1 Personnel

Project manager/engineer:	D. J. White	d.j.white@rl.ac.uk
Customer:	A. R. Weidberg	t.weidberg1@physics.ox.ac.uk

4.2 Deliverables

Project documentation. Data sheet. Test results. Application notes. Tested devices.

4.3 Project plan

Milestones, schedule, see 4.4.

Design and layout will be started after PDR.

AMS 0.8 μ m BICMOS MPW run. 12-channel submission date 24th September 1999.

4.4 Design Reviews

Preliminary Design Review (PDR) to confirm Project Specification held 23rd October 1998.

FDR for the 12-channel version held 9th September 1999.

Concluding Review (CR) and Maintenance Review (MR) to be held after delivery and test.

4.5 Training

Minimal training requirements.

4.6 CAE and test equipment

Workstation, software and support, to suit selected process.

Test equipment as defined in test plan.

4.7 Costs and finance

Based on previous quotes from AMS, 20 prototype 12-channel chips will cost approximately 5k pounds. Packaging and test components unlikely to cost more than 1k pounds per iteration. Requisitions for items on which VAT may be recovered must be authorised by B. T. Payne.

4.8 IPR and confidentiality

Instrumentation Department owns the layout and schematic databases. Any masks or phototools will be procured by the Department. None of these items will be released unless the appropriate protective agreements are in place.

4.9 Safety

Low voltage, low power circuitry, no particular hazards associated with this device. DRX may be fully tested electrically. Laser safety may become a problem for system tests and final use.

4.10 Environmental impact

A small amount of inert material that may be safely disposed of as landfill.

Appendix 1

Power Budget Calculations: A. R. Weidberg.

Minimum coupled power into 50/125u fibre for MITEL VCSEL in GEC package = 300uW.

Losses in the transmission are given below:

Effect	Loss (dB)
Operating temperature of VCSEL	-0.8
Attenuation of 90m fibre	0.22
Radiation damage Fujikura fibre	0.2
Radiation damage Plasma fibre	0.3
MT PPB1/PPF1	0.8
MT PPB2/PPF2	3.0
Total attenuation	3.72

Minimum optical signal = 127uW

Minimum PIN responsivity = 0.45 A/W

Minimum signal current = 57uA