Project Specification

Project Name: VDC

Version: 1.0

Approval:

	name	signature	date
Project Manager	**D. J. White**	**D. J. White**	**29/07/98**

Distribution for all updates:

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Design Support Group Leader:
Management Support Services Group Leader:
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1.0 Scope

To design a modified version of the dual LED Driver Circuit (LDC). This version will have lower drive current to suit VCSELs rather than LEDs. The circuit will be designed with more voltage "headroom" on the output device to allow for the higher "on" voltage of VCSELs.

2.0 Related projects and documents

ABC (Atlas Binary Chip) Project Specification, D. A. Campbell, RAL.
Biphase Mark Encoder and LED Drive Control Chip, R. L. Wastie, Oxford Nuclear Physics.
DORIC4 Project Specification, D. J. White, RAL.
LDC Project Specification, D. J. White, RAL.
Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI). Draft 1.3 IEEE P1596.3-1995.
Performance of VCSELs for SCT Links, I. Mandic and A. Weidberg, Oxford Univ.

3.0 Technical Aspects

3.1 Requirements

3.1.1 General Description

VDC must have two completely independent VCSEL driver circuits on one chip.

3.1.2 Input Signal Requirements

Inputs must be made compatible with LVDS specifications.

3.1.2 Output Requirements

Output current to be made variable from 0 to 20mA, current to be controlled by an external voltage. Starting from +1.6V output current is +4mA/V. A standing current of 1mA ± 0.5mA must be provided to dc bias the VCSEL and improve its switching speed. A resistor is the simplest and best method of providing the standing current because it has a damping effect which helps to minimise ringing of the output waveform. The electrical output should have rise and fall times (10% - 90%) between 0.5ns and 2ns; nominally 1ns. The "on" voltage of a VCSEL may be up to 2.5V at 20mA.

3.1.3 General Requirements

VDC will be required to operate at ambient temperatures up to 30°C during test and down to as low as -15°C when in use on the experiment.
Supply voltage nominally +4V±5%. VDC must withstand an overvoltage of at least 2V without damage and function correctly with minimal decoupling or other external components over the specified temperature and nominal supply voltage ranges.
Any bond pads which may be connected to long lines or to other modules by connectors should aim for electrostatic discharge (ESD) protection to IEC 801-2 compliance level 2, or higher. The signal input protection diodes will be doubled in size compared to LDC to improve the level of protection.

It may not be possible to achieve a high degree of protection on all bond pads for reasons of noise or capacitance loading.
All bond pads to be made as well protected as possible. Careful handling may be needed to prevent damage to sensitive pads during assembly.

3.1.4 Physical Requirements

Chip width must be 1.5mm, chip length 2.5mm, to fit into available space. VCSEL connections at one end, all other connections at the other end. Pad layout to be the same as previous LED driver circuit, figure 1.

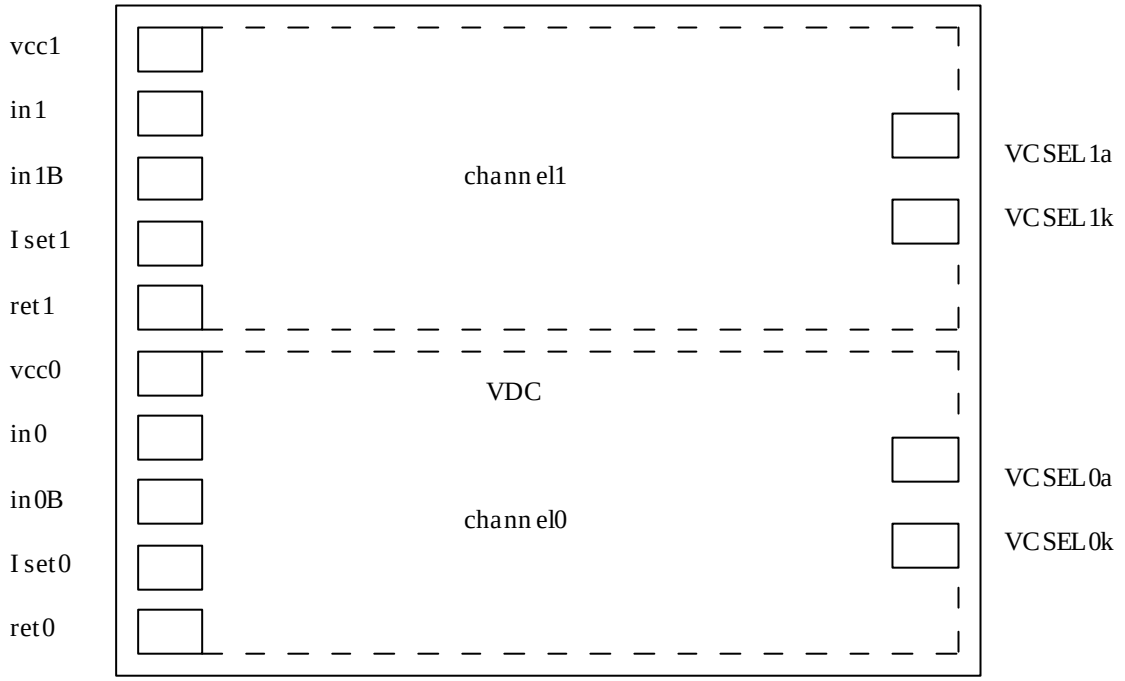

Figure 1. Pad layout and naming.

3.1.5 Pad Numbering and Names

Pads are numbered in an anticlockwise direction starting at vcc1.

Pad#	Pad Name	Function
1	vcc1	supply 1, +4V
2	in1	LVDS input 1 true
3	in1B	LVDS input 1 complement
4	Iset1	VCSEL 1 drive current set
5	ret1	supply 1 return, 0V
6	vcc0	supply 0, +4V
7	in0	LVDS input 0 true
8	in0B	LVDS input 0 complement
9	Iset0	VCSEL 0 drive current set
10	ret0	supply 0 return, 0V
11	VCSEL0k	VCSEL 0 cathode drive

12	VCSEL0a	VCSEL 0 anode drive (vcc0)
13	VCSEL1k	VCSEL 1 cathode drive
14	VCSEL1a	VCSEL 1 anode drive (vcc1)

The supply returns ret0 and ret1 are connected together internally and both are connected to the common substrate. The term 'supply return' is used in preference to 'ground' because there is no effective or common ground for this front end circuitry.
VCSEL outputs are referenced to supply voltage, they must not be shorted to return because excess current will damage the chip or bond wires.

3.2 Specification of deliverables

See Requirements.

3.3 Manufacturing

The circuitry will be designed using AMS 0.8µm BICMOS models and design rules for fabrication on an AMS MPW run. Submission date, 25th September 1998.
This process is not qualified as radiation hard but, if transistors are limited to npn bipolars only and if the circuitry is designed to minimise and to allow for degradation, it should produce sufficiently radiation tolerant devices.

3.4 Testing and product control

Test requirements will be discussed at IDR. A test plan will be written.

3.5 Shipping and Installation

The customer will personally collect all of the deliverables.

3.6 Maintenance and further orders

All documentation will be kept for a period to be determined at Maintenance Review to facilitate maintenance and further orders.

4.0 Project Management

4.1 Personnel

Project manager:	D. J. White	david.white@rl.ac.uk
Project engineer:	D. J. White	david.white@rl.ac.uk
Engineer:	D. J. White	david.white@rl.ac.uk
Customer:	A. R. Weidberg	t.weidberg1@physics.ox.ac.uk

4.2 Deliverables

Project documentation. Test results. Application notes. Tested and untested die.

4.3 Project plan

Milestones, schedule, see 4.4.
Design and layout started after PDR.
AMS 0.8µm BICMOS MPW submission, 25th September 1998.
Testing to be discussed at IDR, test fixtures to be built for January 1999.
Tested die required for use by February 1999.

4.4 Design Reviews

Preliminary Design Review (PDR) to confirm Project Specification,
held on 29th July 1998.
Interim Design Review (IDR) to review project progress and test requirements. Optimistically to be arranged for August 1998.
Final Design Review (FDR) to confirm the devices as designed meet requirements of Project Specification, including any change orders. Planned for late August 1998.
Concluding Review (CR) and Maintenance Review (MR) after delivery.

4.5 Training

Minimal training requirements.

4.6 CAE and test equipment

Workstation, software, support, to suit selected process.
Probe card and test equipment as defined in test plan.

4.7 Costs and finance

Based on previous quote from AMS, cost for 20 prototype chips is ~£2400. An extra 80 may be ordered for ~£1500.
Probe card and test components unlikely to cost more than £3k.
All requisitions to be authorised by M Edwards for items on which VAT may be recovered.

4.8 IPR and confidentiality

Technology Department owns the layout and schematic databases. Any masks or phototools will be procured by the Department. None of these items will be released unless the appropriate protective agreements are in place.

4.9 Safety

Low voltage, low power circuitry, no particular hazards associated with this project.

4.10 Environmental impact

Very little from final product.
Small amounts of inert substance which may be safely disposed of as landfill.

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