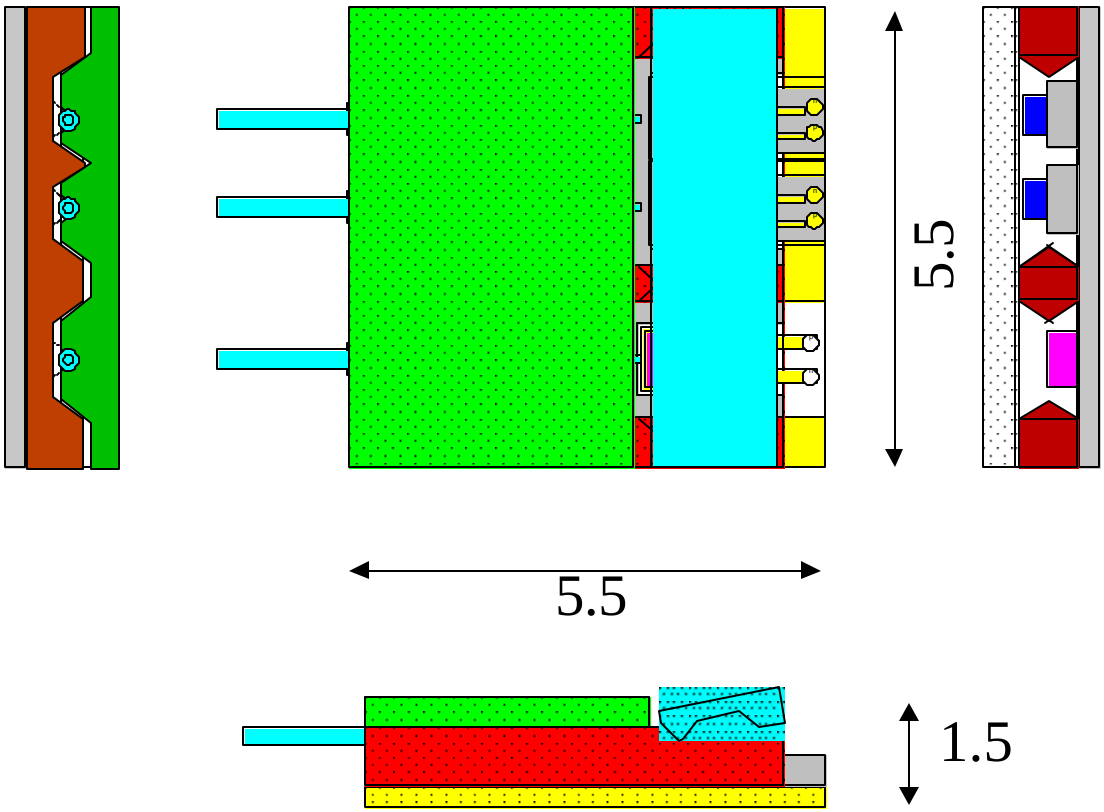
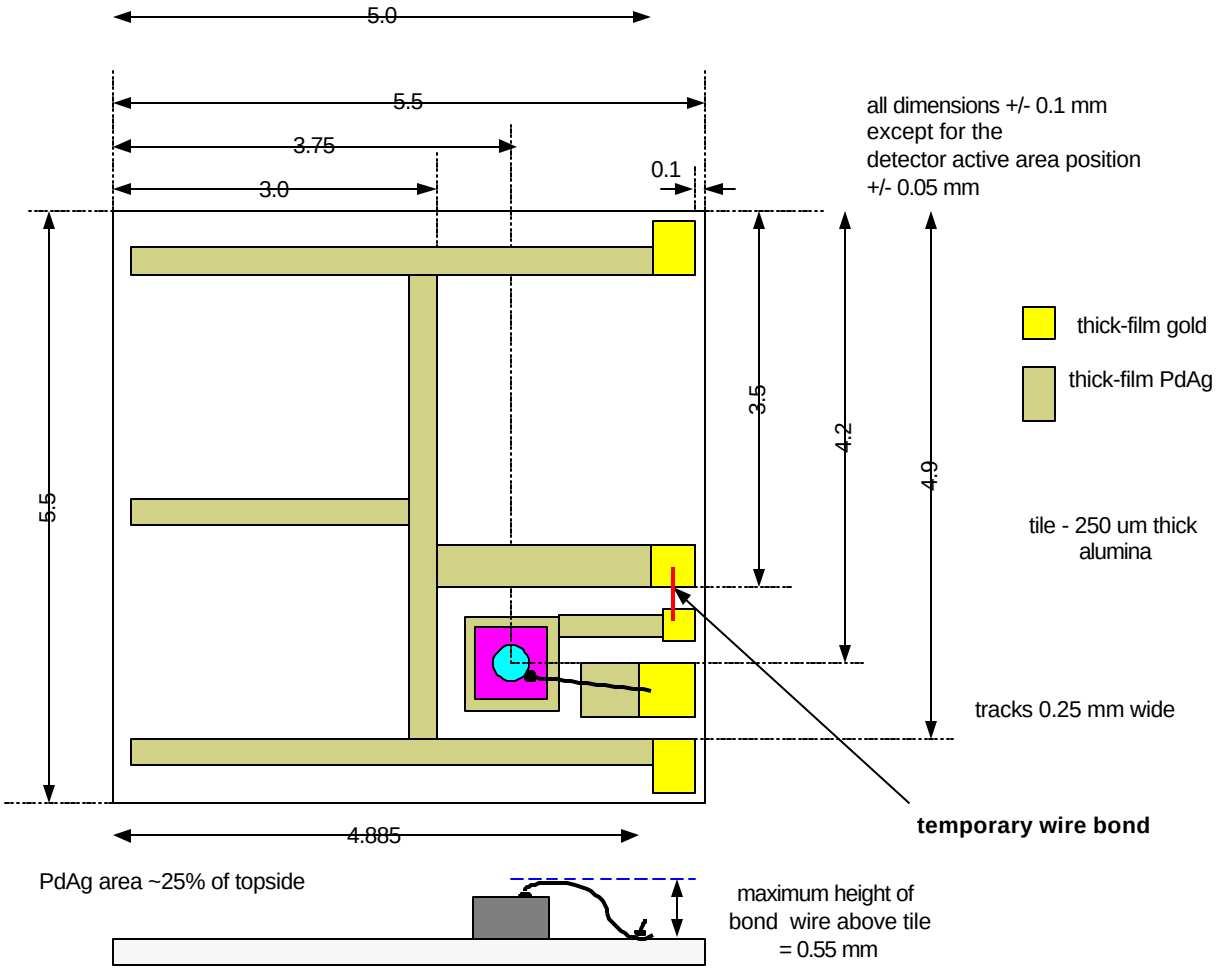
Silicon packaged VCSEL – proposed outline

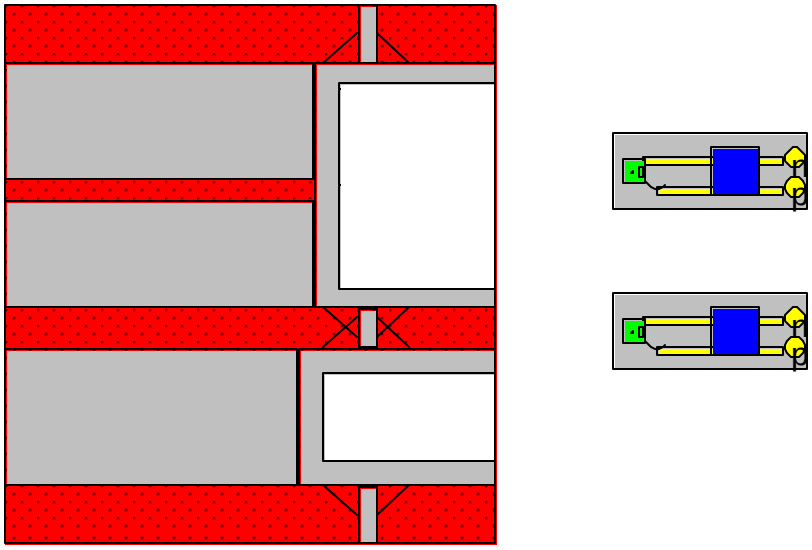


Dimensioned sketch showing main features of the assembly.

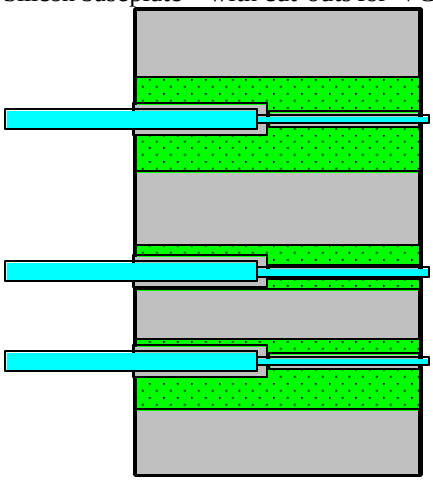
Prepared by Jon Hall, 18.3.99

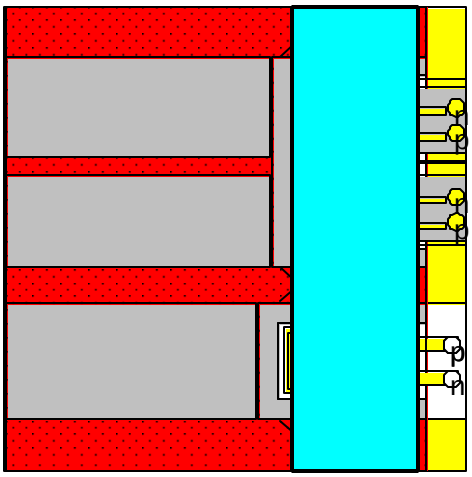
Detector tile - schematic showing proposed metallisation – updated by J. Hall 5.8.99 to have top-side metallisation only – for manufacture by thick-film process (or with ~4 micron thin-film gold) - Marconi Materials Technology, Caswell





Silicon baseplate – with cut-outs for VCSEL carriers (2) and detector





Silicon lid (with v-grooves and fibres) and baseplate / tile / mirror assembly